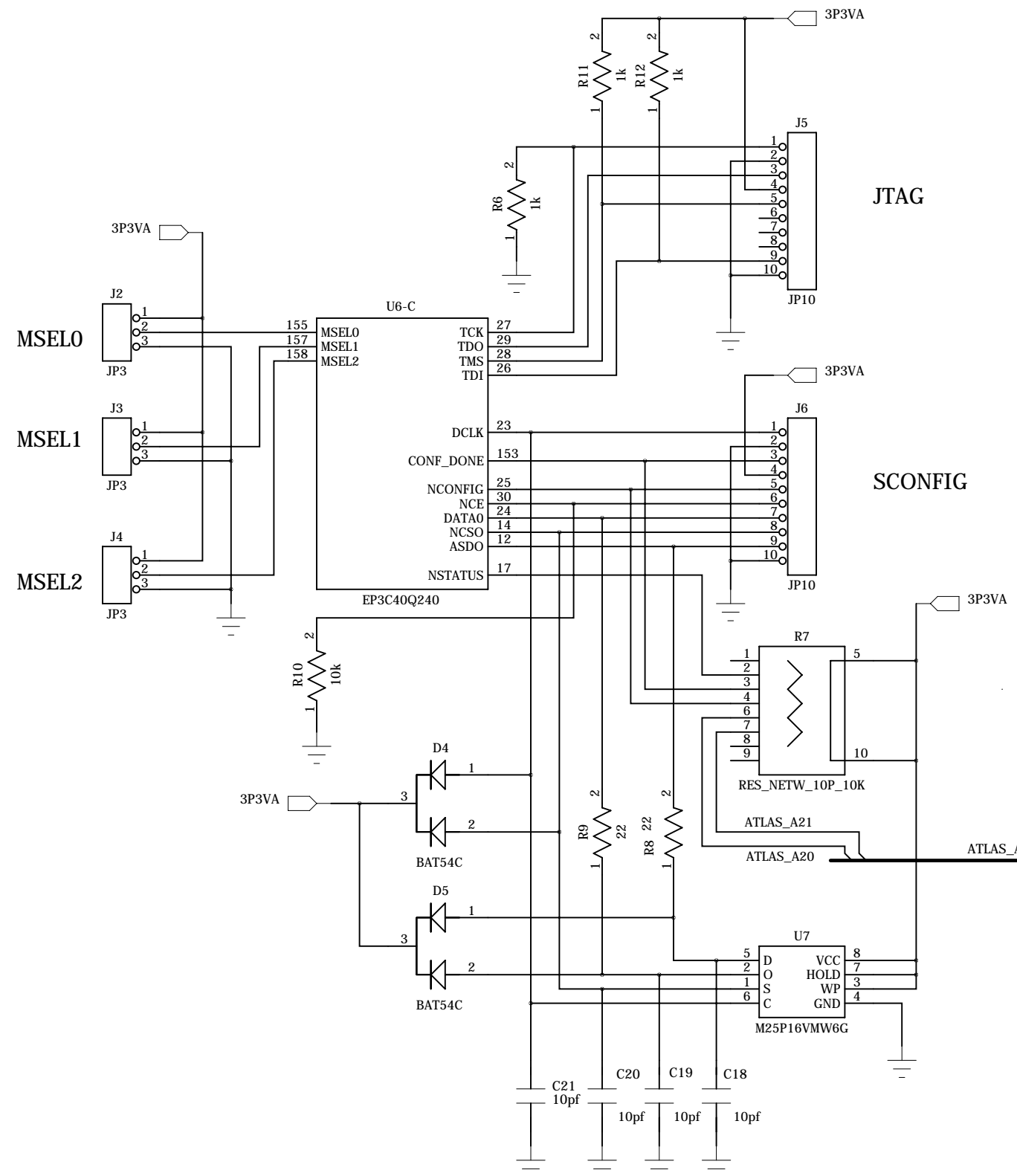
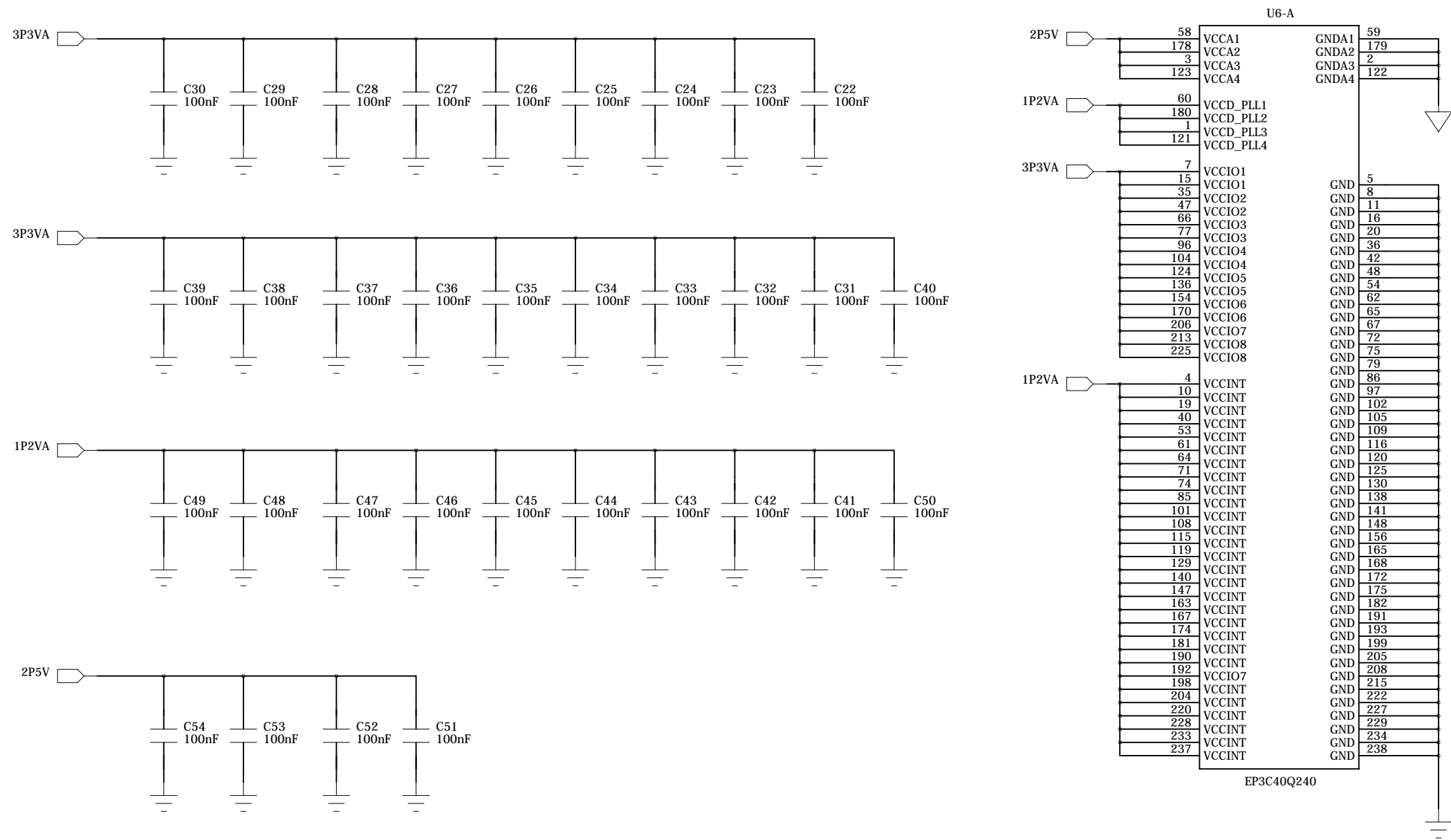
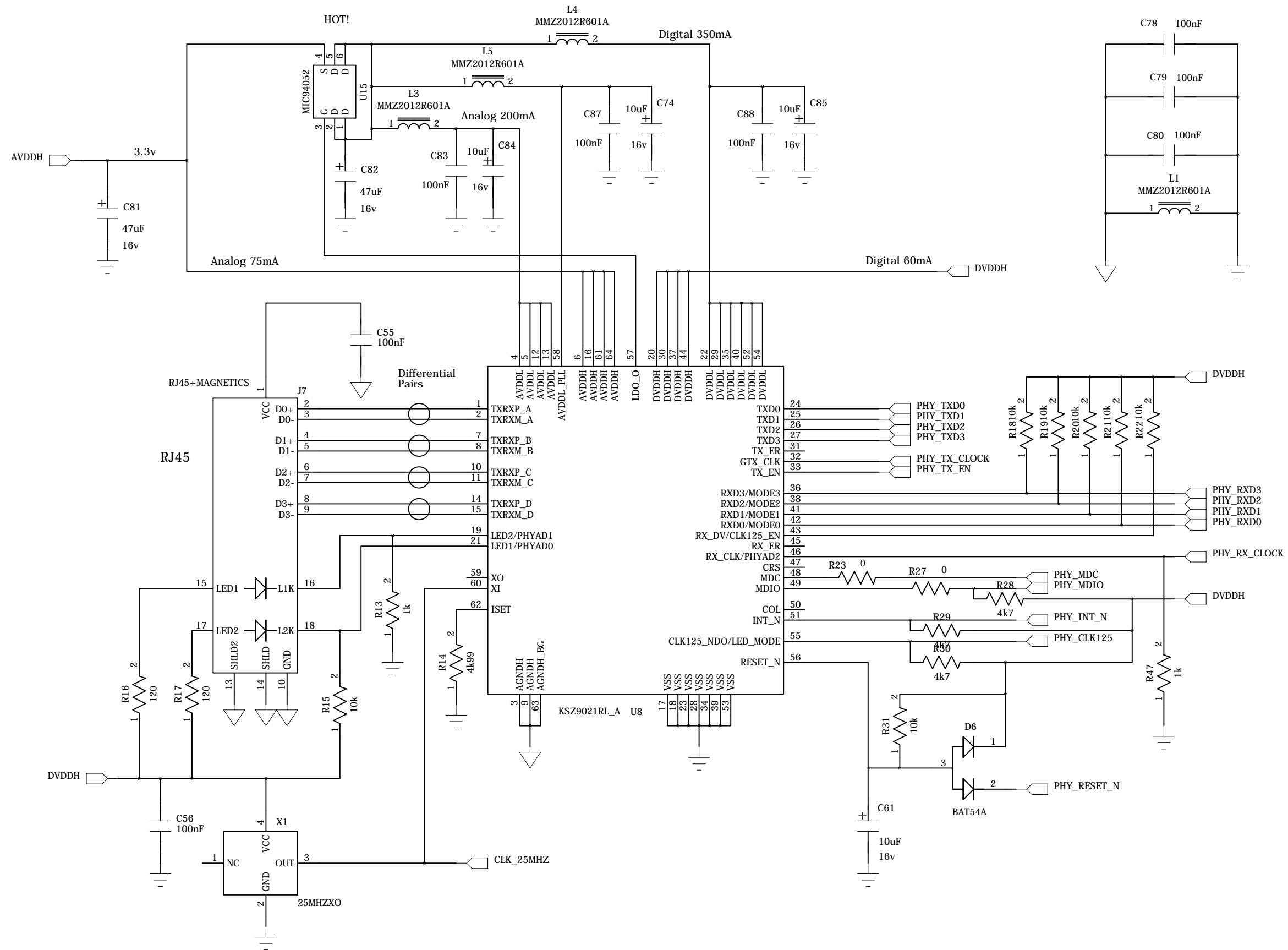


	MSEL2	MSEL1	MSEL0
AS	0	1	0
PS	1	0	0
FPP	1	1	0
JTAG	X	X	X

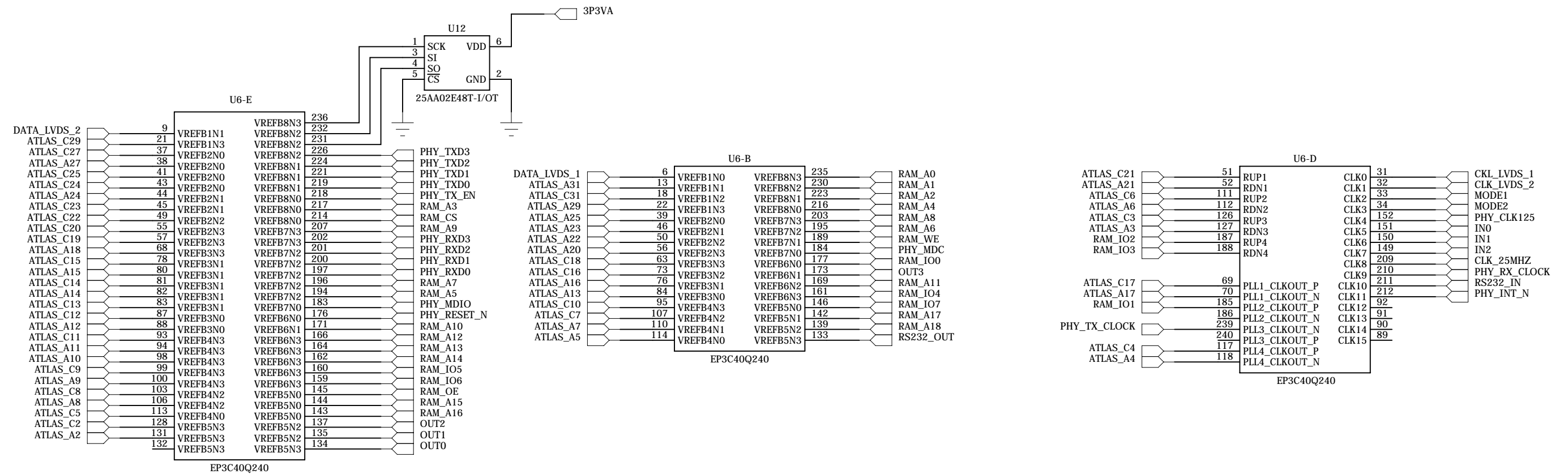






FPGA pin 1 top left

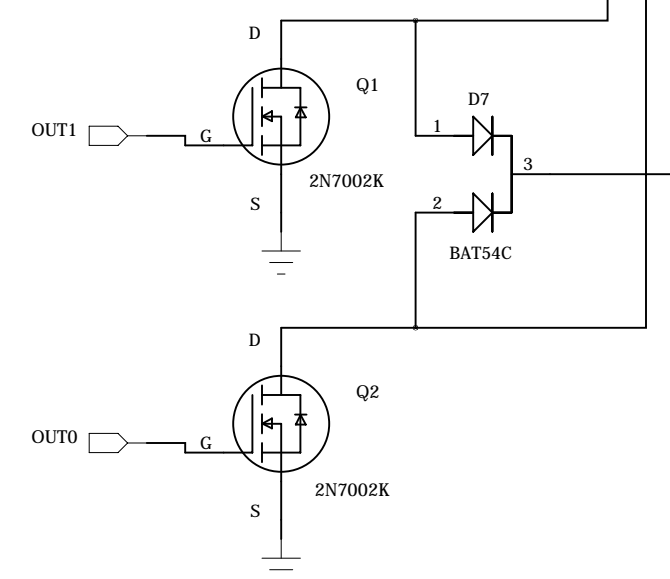
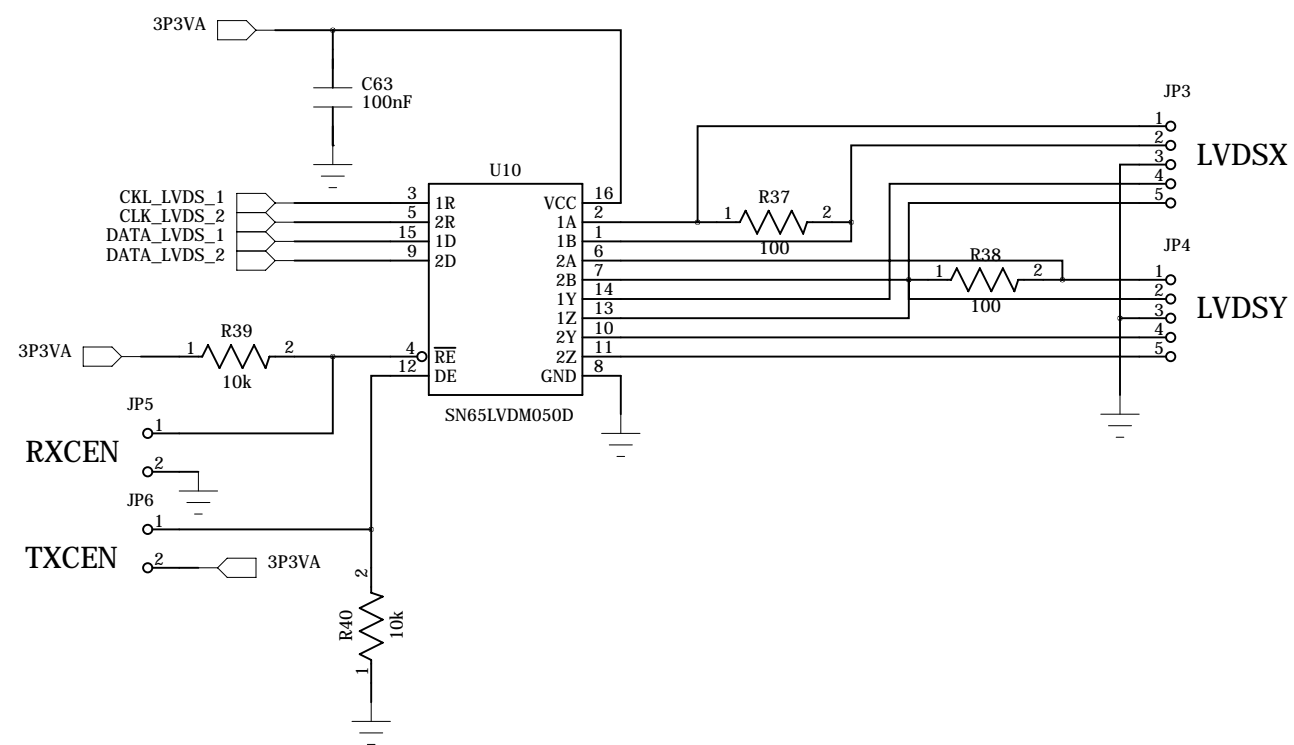
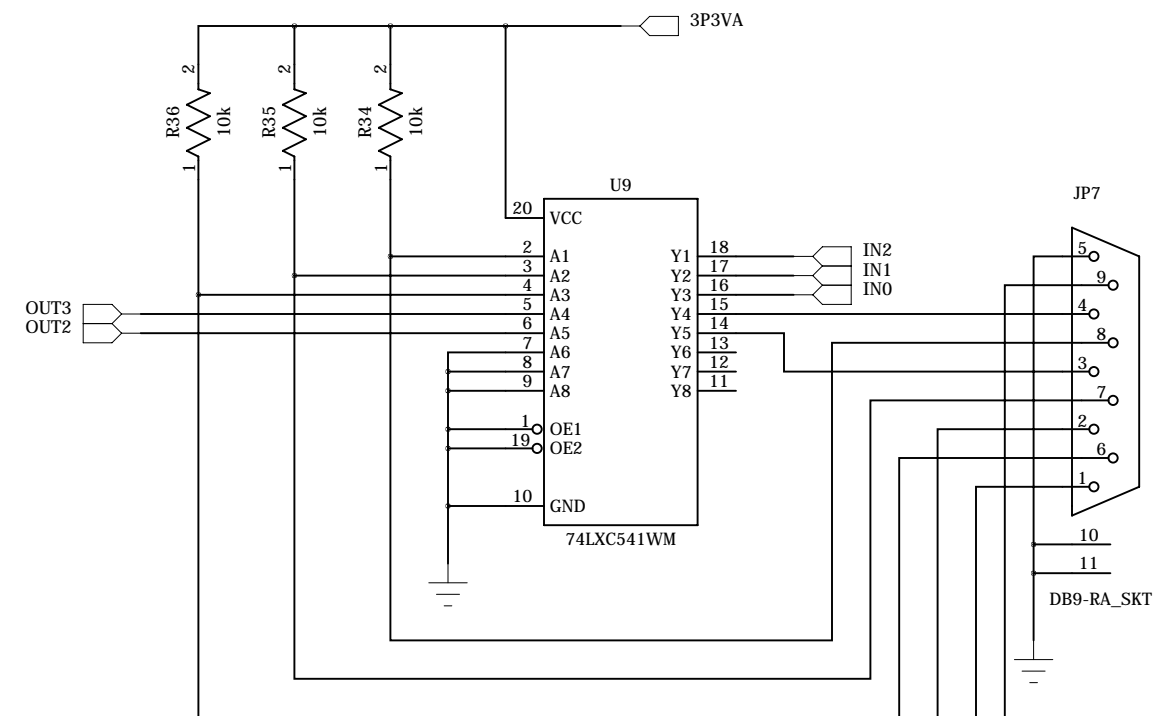
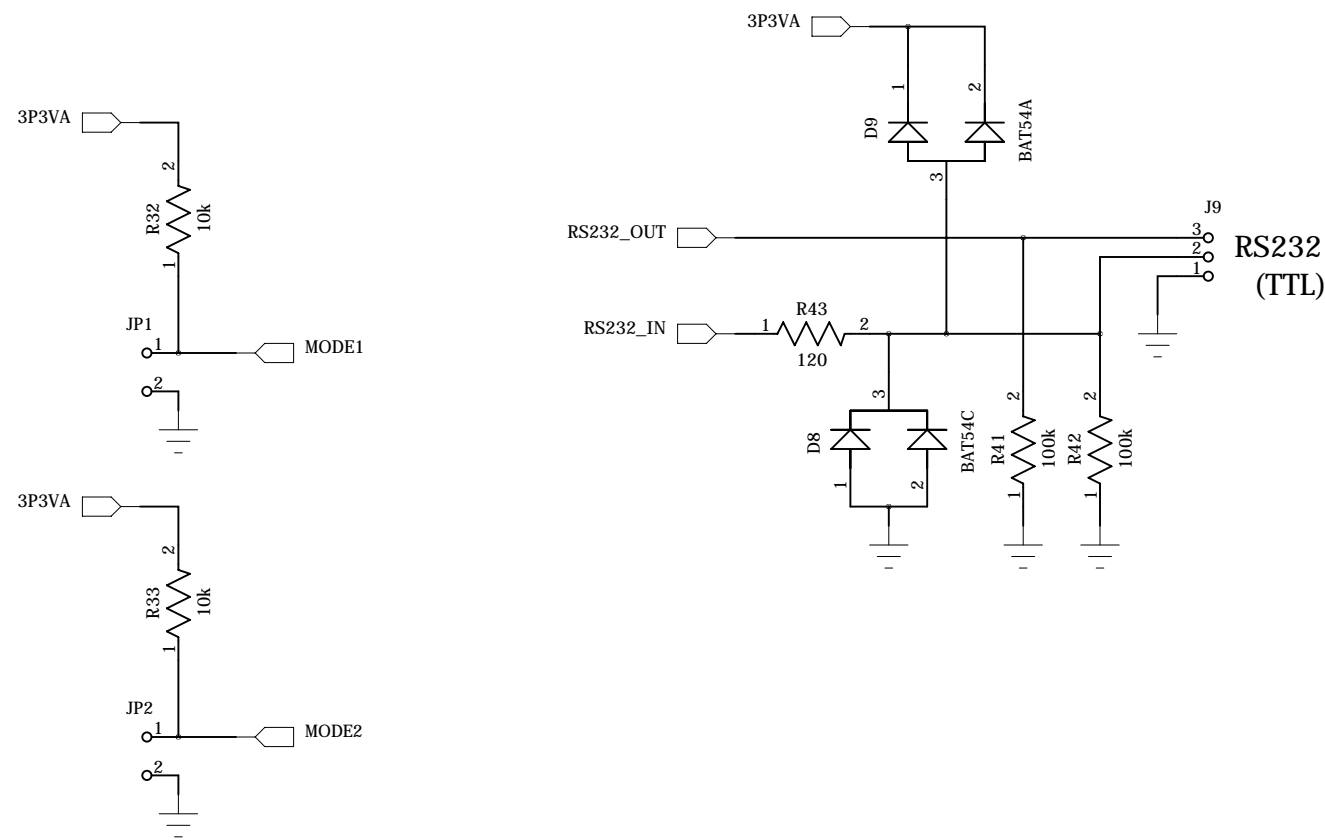
PHY pin 1 bottom right



OpenHPSDR

<FPGA IO>

<OzyII>



OpenHPSDR

<User IO>

<OzyII>

